Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1. (Original) A magnetic random access memory cell, comprising:

first and second sub-digit lines disposed over a semiconductor substrate, the first and second sub-digit lines being spaced apart from each other when viewed from a top plan view; and

a magnetic resistor disposed over the first and second sub-digit lines and overlapping with the first and second sub-digit lines, wherein the magnetic resistor is electrically connected to a predetermined region of the semiconductor substrate through a magnetic resistor contact hole that penetrates a gap region between the first and second sub-digit lines.

2. (Original) A magnetic random access memory cell according to Claim 1, wherein the magnetic resistor has a length and a width smaller than the length when viewed from a top plan view, and the magnetic resistor is disposed to cross over the first and second sub-digit lines along the length thereof.

3. (Original) A magnetic random access memory cell according to Claim 1, wherein the first and second sub-digit lines extend parallel to each other.

4. (Original) A magnetic random access memory cell according to Claim 3, wherein a direction of a current flowing in the first sub-digit line is identical to a direction of a current flowing in the second sub-digit line.

5. (Currently Amended) ~~A magnetic random access memory cell according to Claim 1,~~ A magnetic random access memory cell, comprising:

first and second sub-digit lines disposed over a semiconductor substrate, the first and second sub-digit lines being spaced apart from each other when viewed from a top plan view; and

a magnetic resistor disposed over the first and second sub-digit lines, wherein the magnetic resistor is electrically connected to a predetermined region of the semiconductor substrate through a magnetic resistor contact hole that penetrates a gap region between the first and second sub-digit lines and wherein the first and second sub-digit lines extend parallel to each other and contact each other beyond the magnetic resistor, to form a single merged digit line -having an opening beneath the magnetic resistor, and wherein the magnetic resistor contact hole penetrates the opening.

6. (Original) A magnetic random access memory cell according to Claim 5, wherein the magnetic resistor has a length and a width less than the length when viewed from a top plan view, and the magnetic resistor is disposed to cross over the first and second sub-digit lines along the length thereof.

7. (Original) A magnetic random access memory cell according to Claim 6, wherein the width of the magnetic resistor is less than a length of the opening parallel to the merged digit line.

8. (Original) A magnetic random access memory cell according to Claim 1 further comprising a bit line which is disposed over the magnetic resistor and is electrically connected to the magnetic resistor, wherein the bit line is disposed to cross over the sub-digit lines.

9. (Original) A magnetic random access memory cell according to Claim 1, wherein the magnetic resistor comprises a magnetic tunnel junction including a pinning layer, a pinned layer, a tunneling layer and a free layer which are sequentially stacked, and the pinned layer and the free layer comprise ferromagnetic layers having magnetic spins arrayed in a horizontal direction.

10. (Original) A magnetic random access memory cell, comprising:

an access MOS transistor at a predetermined region of a semiconductor substrate;

first and second parallel sub-digit lines disposed over the access MOS transistor;

a magnetic resistor disposed over the first and second sub-digit lines to overlap with the first and second sub-digit lines, the magnetic resistor being electrically connected to a drain region of the access MOS transistor through a magnetic resistor contact hole that penetrates a gap region between the first and second sub-digit lines; and

a bit line disposed over the magnetic resistor and electrically connected to the magnetic resistor, wherein the bit line crosses over the first and second sub-digit lines.

11. (Original) A magnetic random access memory cell according to Claim 10 further comprising a common source line electrically connected to a source region of the access MOS transistor, wherein the common source line extends parallel to the sub-digit lines.

12. (Original) A magnetic random access memory cell according to Claim 10, wherein a direction of a current flowing in the first sub-digit line is identical to a direction of a current flowing in the second sub-digit line.

13. (Original) A magnetic random access memory cell according to Claim 10 further comprising spacers and capping layers covering the sidewalls and top surfaces of the sub-digit lines respectively, wherein the magnetic resistor contact hole extends between adjacent spacers and between the capping layers.

14. (Original) A magnetic random access memory cell according to Claim 10, wherein the magnetic resistor has a length and a width less than the length when viewed from a top plan view and the magnetic resistor is disposed to cross over the first and second sub-digit lines along the length thereof.

15. (Original) A magnetic random access memory cell according to Claim 10, wherein the magnetic resistor comprises a magnetic tunnel junction including a pinning layer, a pinned layer, a tunneling layer and a free layer which are sequentially stacked, and the pinned layer and the free layer comprise ferromagnetic layers having magnetic spins arrayed in a horizontal direction.

16. (Withdrawn) A magnetic random access memory cell, comprising:

an access MOS transistor at a predetermined region of a semiconductor substrate;

a merged digit line disposed over the access MOS transistor, the merged digit line having an opening in a predetermined region thereof;

a magnetic resistor disposed over the opening to overlap with the merged digit line, the magnetic resistor being electrically connected to a drain region of the access MOS transistor through a magnetic resistor contact hole that penetrates the opening; and

a bit line disposed over the magnetic resistor and electrically connected to the magnetic resistor, the bit line being disposed to cross over the merged digit line.

17. (Withdrawn) A magnetic random access memory cell according to Claim 16 further comprising a common source line electrically connected to a source region of the access MOS transistor, wherein the common source line extends parallel to the merged digit line.

18. (Withdrawn) A magnetic random access memory cell according to Claim 16 further comprising a spacer and a capping layer covering a sidewall of the opening and a top surface of the merged digit line respectively, wherein the magnetic resistor contact hole extends inside the spacer and the capping layer.

19. (Withdrawn) A magnetic random access memory cell according to Claim 16, wherein the magnetic resistor has a length and a width less than the length when viewed from a top plan view, and the magnetic resistor is disposed to cross over the merged digit line along the length thereof.

20. (Withdrawn) A magnetic random access memory cell according to Claim 19, wherein a width of the magnetic resistor is less than a length of the opening parallel to the merged digit line.

21. (Withdrawn) A magnetic random access memory cell according to Claim 16, wherein the magnetic resistor comprises a magnetic tunnel junction including a pinning layer, a pinned layer, a tunneling layer and a free layer which are sequentially stacked, and the pinned layer and the free layer comprise ferromagnetic layers having magnetic spins arrayed in a horizontal direction.

22. (Currently Amended) A Magnetic Random Access Memory (MRAM) cell comprising:

an MRAM substrate;

a magnetic resistor on the MRAM substrate; and

first and second digit lines between the magnetic resistor and the MRAM substrate and extending beneath the magnetic resistor, wherein the magnetic resistor overlaps the first and second digit lines.

23. (Original) An MRAM cell according to Claim 22, further comprising a magnetic resistor contact plug that electrically contacts the magnetic resistor and extends from the magnetic resistor towards the MRAM substrate, between the first and second digit lines.

24. (Original) An MRAM cell according to Claim 23 further comprising first and second sidewall spacers, a respective one of which is on a sidewall of the respective first and second digit lines and face one another, and wherein the magnetic resistor contact plug extends between the first and second sidewall spacers.

25. (Currently Amended) A Magnetic Random Access Memory (MRAM) cell comprising:

an MRAM substrate;

a magnetic resistor on the MRAM substrate; and

first and second digit lines between the magnetic resistor and the MRAM substrate and extending beneath the magnetic resistor, ~~An MRAM cell according to Claim 22~~ wherein the first and second digit lines merge into a single digit line beyond the magnetic resistor.

26. (Original) An MRAM cell according to Claim 22 wherein the magnetic resistor is an elongated magnetic resistor having a length that is greater than a width thereof, and wherein the magnetic resistor extends across the first and second digit lines along the length thereof.

27. (Currently Amended) A Magnetic Random Access Memory (MRAM) cell comprising:

an MRAM substrate;

a magnetic resistor on the MRAM substrate;

first and second digit lines between the magnetic resistor and the MRAM substrate and extending beneath the magnetic resistor; and ~~An MRAM cell according to Claim 22~~

~~further comprising~~ a merged digit line between the magnetic resistor and the MRAM substrate, extending beneath the magnetic resistor and including therein a hole beneath the magnetic resistor that defines the first and second digit lines beneath the magnetic resistor.

28. (Original) An MRAM cell according to Claim 23 further comprising a transistor in the MRAM substrate and electrically connected to the magnetic resistor contact plug.

29. (Original) An MRAM cell according to Claim 22 wherein the first and second digit lines are electrically connected in parallel.